ABSTRACT OF THE DISCLOSURE

The present invention relates to a base pad layout for reducing the parasitic base-collector capacitance and method of fabricating HBT using the same.

The present invention comprises a base region which is aligned in a <01$\bar{1}$> or <011> orientation with respect to the semiconductor substrate; a base pad region which has a fixed slope with respect to said base region; and a base feeding region which is aligned in a <010> orientation and connects said base region and said base pad region.

According to the present invention, the base-collector capacitance due to base pad could be reduced through a simple base pad layout and wet etching which isolates an active base region and a base pad region.

The present invention uses the conventional wet etching method for fabricating a triple mesa HBT involving only a modification of the base pad layout, hence, no additional process is required.